WHAT IS CLAIMED IS:

1. A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:

providing a substrate;

forming a gate insulation layer and a conductive layer over the substrate sequentially;

performing a pre-amorphization implantation on the conductive layer so that the conductive layer is amorphized, wherein the pre-amorphization implantation is carried out using a dopant having an ionic radius greater than a germanium ion;

patterning the conductive layer and the gate insulation layer to form a gate structure;

forming a first spacer on the sidewalls of the gate structure;

forming a doped source/drain extension region in the substrate on each side of the first spacer;

forming a second spacer on the sidewall of the first spacer;

forming a doped source/drain region in the substrate on each side of the second spacer; and

performing a solid phase epitaxial process to re-crystallize the amorphized conductive layer in the gate structure and activate the dopants in the doped source/drain extension region and the doped source/drain region to form a source/drain terminal.

2. The method of claim 1, wherein the dopants comprise xenon, argon or krypton ions.

3. The method of claim 2, wherein the pre-amorphization implantation is carried out using the dopants set to a dosage level in a range of $1*10^{14}$ to $5*10^{14}$ atoms/cm^2.

4. The method of claim 2, wherein the pre-amorphization implantation is carried out using the dopants accelerated to an energy level in a range of 25 to 70 KeV.

5. The method of claim 1, wherein a deposition temperature of a dielectric layer for forming the second spacer is in a range of 500°C~650°C.

6. The method of claim 5, wherein the method for forming the second spacer comprise using a BTBAS (Bis(tert-butylamino)silane) as a precursor to carry out the deposition of the dielectric layer for forming the second spacer.

7. The method of claim 1, wherein after the step of performing the pre-amorphization implantation, furthermore includes performing an ion implantation process to convert the conductive layer into an N-type or P-type conductive layer.

8. A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:

providing a substrate having a gate structure thereon;

forming a first spacer on the sidewalls of the gate structure;

performing a pre-amorphization implantation to amorphize a portion of the substrate, wherein the amorphization implantation is carried out using a dopant having an ionic radius greater than a germanium ion;

forming a doped source/drain extension region in the substrate on each side of the first spacer;

forming a second spacer on the sidewall of the first spacer;

forming a doped source/drain region in the substrate on each side of the second spacer; and performing a solid phase epitaxial process to re-crystallize the amorphized portion of the substrate and activate the doped source/drain extension region and the doped source/drain region to form a source/drain terminal.

9. The method of claim 8, wherein the dopants comprise xenon, argon or krypton ions.

10. The method of claim 9, wherein the pre-amorphization implantation is carried out using the dopants set to a dosage level in a range of $1*10^{14}$ to $5*10^{14}$ atoms/cm^2.

11. The method of claim 9, wherein the pre-amorphization implantation is carried out using the dopants accelerated to an energy level in a range of 25 to 70 KeV.

12. The method of claim 8, wherein a deposition temperature of a dielectric layer for forming the second spacer is in a range of 500°C~650°C.

13. The method of claim 12, wherein the method for forming the second spacer comprise using a BTBAS (Bis(tert-butylamino)silane) as a precursor to carry out the deposition of the dielectric layer for forming the second spacer.

14. A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:

providing a substrate;

forming a gate insulation layer and a conductive layer over the substrate sequentially;

performing a first pre-amorphization implantation on the conductive layer so that the conductive layer is amorphized, wherein the first pre-amorphization implantation is carried out using a first dopant having an ionic radius greater than a germanium ion;

patterning the conductive layer and the gate insulation layer to form a gate structure;

forming a first spacer on the sidewalls of the gate structure;

performing a second pre-amorphization implantation on the substrate so that a portion of the substrate is amorphized, wherein the second pre-amorphization implantation is carried out using a second dopant having an ionic radius greater than a germanium ion;

forming a doped source/drain extension region in the substrate on each side of the first spacer;

forming a second spacer on the sidewall of the first spacer;

forming a doped source/drain region in the substrate on each side of the second spacer; and

performing a solid phase epitaxial process to re-crystallize the amorphized conductive layer in the gate structure and the amorphized substrate and then activate the dopants in the doped source/drain extension region and the doped source/drain region to form a source/drain terminal.

15. The method of claim 14, wherein the first dopants comprise xenon, argon or krypton ions.

16. The method of claim 15, wherein the pre-amorphization implantation is carried out using the first dopants set to a dosage level in a range of $1*10^{14}$ to $5*10^{14}$ atoms/cm^2.

17. The method of claim 15, wherein the pre-amorphization implantation is carried out using the first dopants accelerated to an energy level in a range of 25 to 70 KeV.

18. The method of claim 14, wherein the second dopants comprise xenon, argon or krypton ions.

19. The method of claim 18, wherein the pre-amorphization implantation is carried out using the second dopants set to a dosage level in a range of $1*10^{14}$ to $5*10^{14}$ atoms/cm^2.

20. The method of claim 18, wherein the pre-amorphization implantation is carried out using the second dopants accelerated to an energy level in a range of 25 to 70 KeV.

21. The method of claim 14, wherein a deposition temperature of a dielectric layer for forming the second spacer is in a range of 500°C~650°C.

22. The method of claim 21, wherein the method for forming the second spacer comprise using a BTBAS (Bis(tert-butylamino)silane) as a precursor to carry out the deposition of the dielectric layer for forming the second spacer.

23. The method of claim 14, wherein after the step of performing the first pre-amorphization implantation, furthermore includes performing an ion implantation process to convert the conductive layer into an N-type or P-type conductive layer.